HÖFT & WESSEL

HW 86010

DECT Transceiver Module

Integration Manual

Version 1.22

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1.00	First official release
1.19	take out firmware description; internal release
1.20	External release
1.21	Added picture on antenna soldering
1.22	Corrections

Table of Contents

1.0 Preface

Dear customer. Thank you for selecting the HW 86010 DECT transceiver module. You have made a good choice, since HW 86010 is a powerful and very versatile product that easily adds DECT communication to your application.

This document will help you in getting the optimum integration result. This covers mechanical, electrical and RF aspects.

Höft & Wessel aims for best customer satisfaction. In case of any problems with this manual or with our products please do not hesitate to contact us. Your feedback will enable our specialists to solve your problems and continually improve our products and documentation.

1.1 About this document

This integration manual contains the full technical specification of the HW 86010 as well as all necessary information for a successful integration.

HW 86010 is a future-proof product which offers a number of flexible interfaces and features. It is delivered together with Höft & Wessel DECT firmware.

This Integration manual is focussed on the description of hardware features. Not all of these possibilities are supported by the standard firmware but some will require a customised firmware. Please always read this Integration manual together with the Firmware manual in order to verify that your desired operation is possible.

1.2 Contact Höft & Wessel AG

For immediate assistance please address yourself to the Höft & Wessel service line:

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Latest revisions of all publicly available documentation and firmware downloads are available from our web-site www.hoeft-wessel.de

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2.0 Product overview

The DECT transceiver module HW 86010 is a highly versatile and powerful engine for popular and advanced DECT applications. It provides both RF and baseband signal processing as well as a complete DECT protocol stack.

2.1 General description

Built around a 55 MHz high-speed µC core the architecture of the HW 86010 features a full set of useful interfaces for best support of voice and data services in various environments.

These include RS-232 for circuit data transmission, PCM interface to connect to standard ISDN or PBX systems, I²C for auxiliary functions and analogue input/output for voice. Additional general purpose I/Os plus an accessible bus interface make the HW 86010 ideally suited for automation and control applications with specific I/O requirements.

The RF section of the HW 86010 comprises a single-blind-slot radio, fully compliant with EN 300 175-2. It offers improved functionality. Three antenna connections allow flexible configurations. E.g. use of two antennas for standard antenna diversity, together with an additional directional antenna. Switching between antennas is performed under software control.

The DECT protocol stack has been implemented as firmware running on the µC of the HW 86010. Please consult your Firmware manual for a detailed description of the Firmware features.

The ultra-compact and low-voltage design make the HW 86010 optimally suited for battery powered devices.

2.2 Architecture

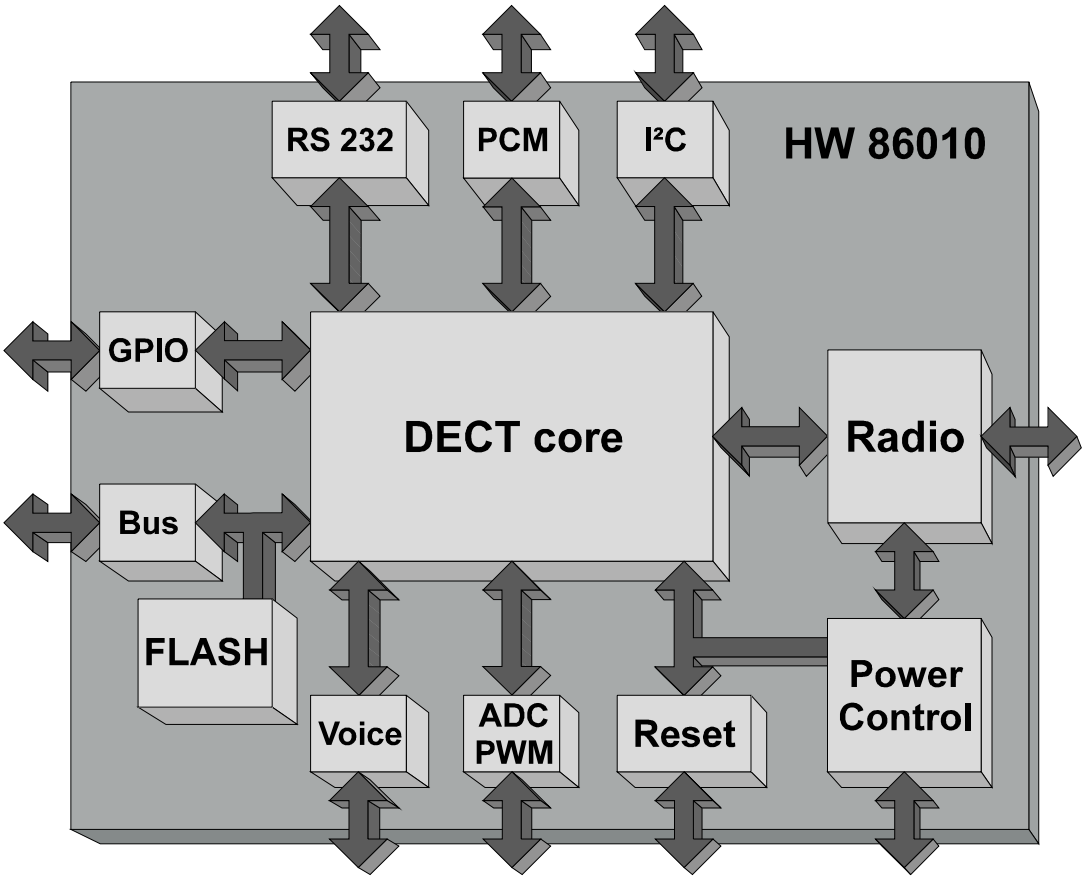


Figure 1: Architecture of DECT transceiver module HW 86010

RS-232	Asynchronous serial interface, full duplex, selectable data rate up to 115,2 kBd
PCM	Isochronous serial interface, IOM-2 compatible, full duplex, maximum clock rate 4,096 MHz, data rate 256 kBd
I²C	Isochronous serial interface used for control of on-board peripherals, half duplex
GPIO	General purpose digital I/O pins
DECT core	Dedicated µC that runs the DECT firmware
Radio	RF section that generates and receives radio signals
Bus	Direct interface to the internal bus of the core µC
FLASH	Non-volatile memory used to store the firmware and parameters
Voice	Interfaces for microphone, speaker and ringer
ADC/PWM	Analogue input and PWM output (used to generate analogue output signals)
Reset	Monitors power supply and resets the module if voltage is too low or external reset input is activated
Power Control	Generates operating voltage for the DECT core and the radio

2.3 Environmental Conditions

2.3.1 Storage Temperature Range

	°C
Nominal	-25 to +75

2.3.2 Operating Temperature Range

	°C
Nominal	+15 to +35
Extreme	-10 to +55

2.3.3 Humidity

	% rel.
Nominal	0 to 90, non-condensing

3.0 Hardware description

3.1 Mechanical characteristics

3.1.1 Dimensions

	mm
Length	53.0, tolerances see section 3.1.3
Width	37.0, tolerances see section 3.1.3
Height	7.2, tolerances see section 3.1.3

3.1.2 Weight

	g
Weight	18 +/- 2

3.1.3 Mechanical drawing

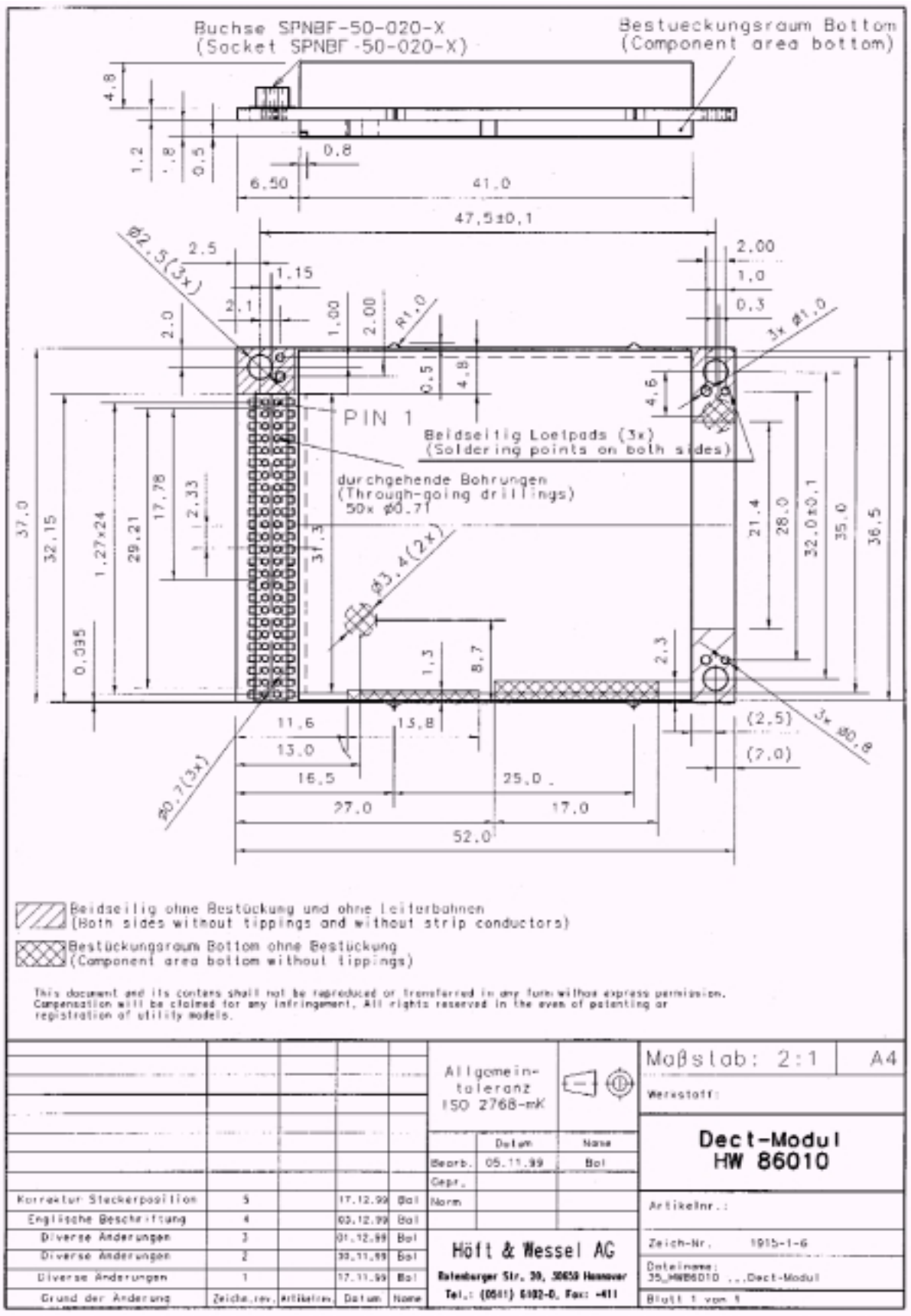


Figure 2: Mechanical drawing

3.1.4 Antenna Assembly

3.1.4.1 Specification of internal wire antenna

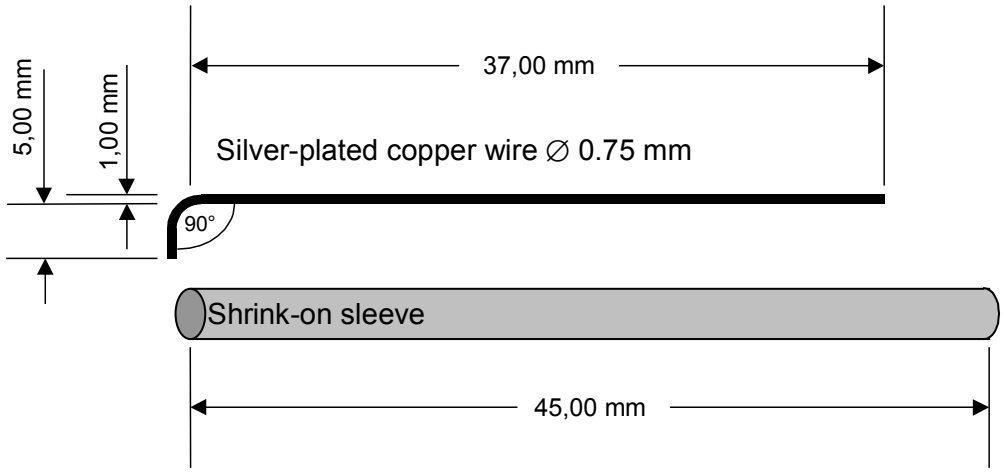


Figure 3: Internal wire antenna

3.1.4.2 Mounting of antennas

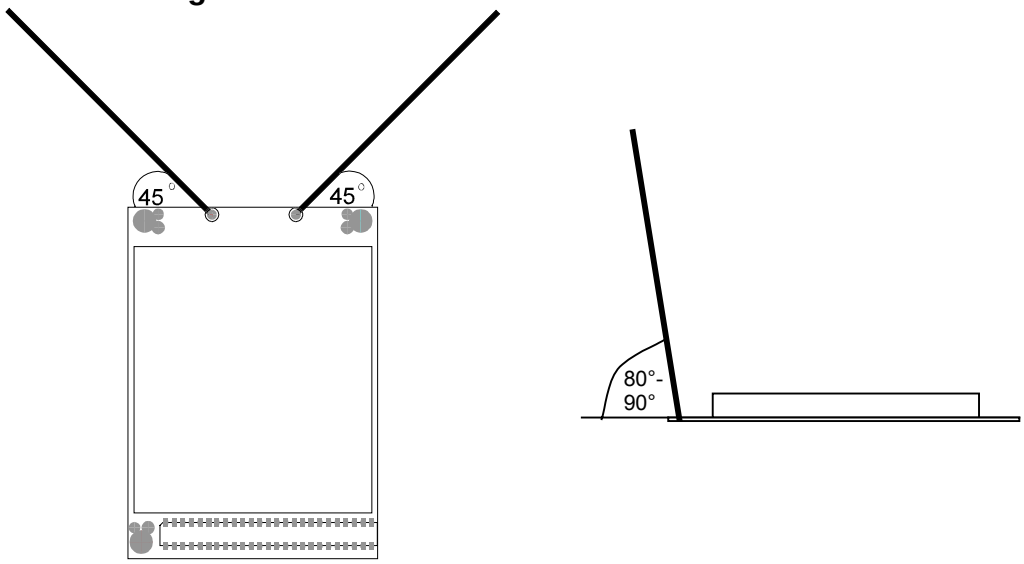


Figure 4: Recommended mountings of internal wire antennas

Caution: Be careful not to shortcut or ground the antennas, since this may damage the HW 86010.

The antennas are DC coupled with the module.

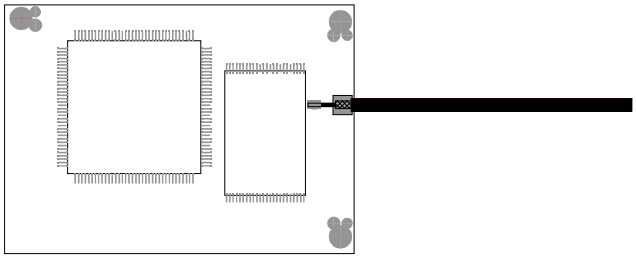


Figure 5: Recommended mounting of external antenna

An external antenna (50Ω impedance) may be connected as indicated.

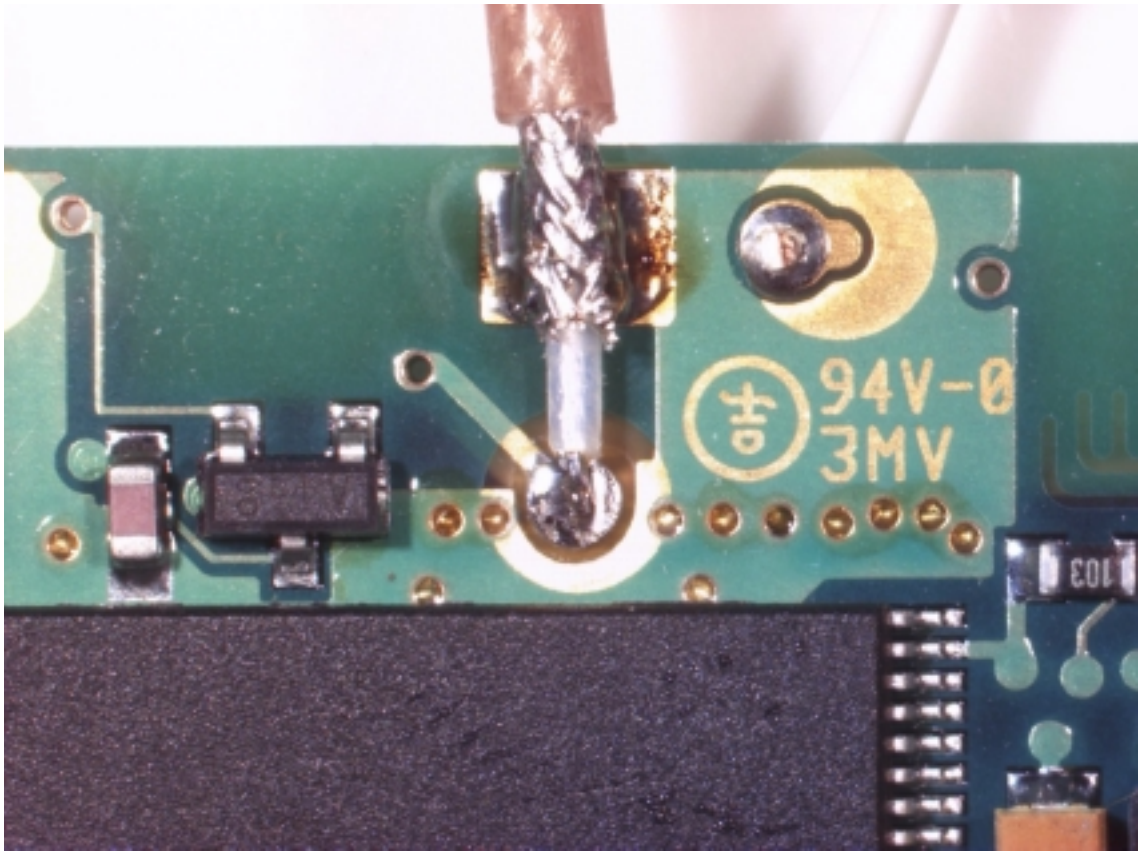


Figure 6: Soldering the external antenna

3.2 Electrical characteristics

3.2.1 Supply voltage V3P3

	min.	max.
Absolute maximum rating	-0.5V	+3.63V
Operating	+3.0V	+3.6V
Ripple		+/-30mV

Voltage V3P3 is used as power supply for the baseband section of HW 86010. It is the reference voltage for all digital I/Os.

The current consumption on V3P3 depends on the power management. Power management only applies to the PT, not to the FT. The PT may enter a sleep mode whilst the FT is always active.

During firmware download the current consumption is higher, because additional power is needed for writing the Flash memory

Mode	average I3P3	peak I3P3
Sleep mode (PT only)	9mA	50mA
Active mode	40mA	50mA
Firmware download	40mA	90mA

All values are approximate figures measured under typical operating conditions (20°C).

3.2.2 Supply voltage VBATP

	min.	max.
Absolute maximum rating	-0.5V	+5.5V
Operating	+3.3V	+4.7V
Ripple		+/-100 mV

Voltage VBATP is used as power supply for the radio section of HW 86010.

Mode	average IBATP	peak IBATP
Sleep mode (PT only)	3mA	300mA
Scan mode (PT only)	60mA	300mA
Idle mode (FT only)	50mA	400mA
1 traffic bearer	50mA	400mA
4 traffic bearers	110mA	400mA

All values are approximate figures measured under typical operating conditions.

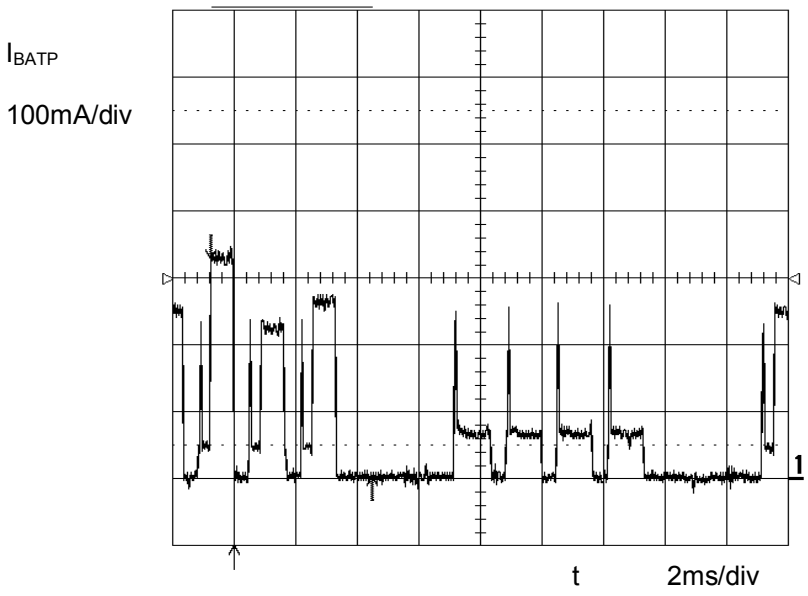


Figure 7: Typical IBATP bursts (multi-bearer connection active)

The current consumption on VBATP depends on the power management and on the number of active traffic bearers. Power management only applies to the PT, not to the FT. The PT may enter a sleep mode whilst the FT is always active. If no communication is active, the FT operates in idle mode. In this mode it sends out a dummy bearer.

Even in sleep mode a PT stays synchronised to the FT. In case synchronisation is lost, the PT scans all DECT channels until it finds a suitable FT. In scan mode the PT requires more power.

Caution: When a PT does not receive a valid FT it enters scan mode. This may reduce stand-by time of battery-powered devices. Try to avoid this situation.

3.2.3 Logical signals

Signal	min.	max.
Logical high output	V3P3 - 0.3V	V3P3
Logical low output	0.0V	+0.5V
Logical high input	0.7 x V3P3	V3P3 + 0.3V
Logical low input	-0.5V	0.3 x V3P3
Iout output logical high		2mA source
Iout output logical low		2mA drain

3.3 Radio specification

Parameter	Values
Frequency range	1880.064MHz to 1898.208MHz
Number of channels	10
Channel spacing	1.728MHz
Frequency offset	± 50kHz at extreme conditions
Modulation	Gaussian Frequency Shift Keying (GFSK: BxT=0.5 ; m= 288kHz)
Multiplexing	Time Division Multiple Access (TDMA)
Bearers per channel	12 full-slot duplex bearers
Number of bearers used at the same time	6
Total system data rate	7.5 Mbit/s at the air interface
Maximum data rate for a single radio	384 kbit/s at the air interface
Data rate per bearer per direction	32 kbit/s at the air interface
Transmitter power	250mW during active transmit slot
Range	inhouse: up to 50m outdoor: up to 300m
Reference timer accuracy	better than 5 ppm at nominal conditions better than 10 ppm at extreme conditions
Packet jitter	<0.1µs
Packet delay variations	<2.0µs at extreme conditions
Receiver sensitivity	-87 dBm typical at 10^{-3} BER
Antennas	2 internal, 1 external antenna
Load impedance	50Ω external antenna

3.4 Interface description

3.4.1 Connector specification

The external interface of the HW 86010 is implemented as 50-pin connector. The connector on the module is compatible to Samtec part number CLP-125-02-G-D-BE.

The recommended way to connect the HW 86010 is bottom-entry, i.e. through the printed circuit board. A suited connector is Samtec FTSH-125-01

The following figures illustrate two preferred mounting scenarios

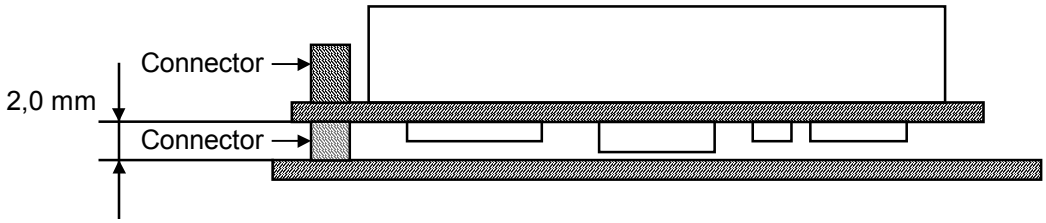


Figure 8: No components fitted on target PCB below HW 86010. Minimum distance between PCBs 2,0 mm

When Samtec FTSH-125-01 is used as mating connector, minimum distance between the PCBs is 2.92mm, as given by the profile of the Samtec connector.

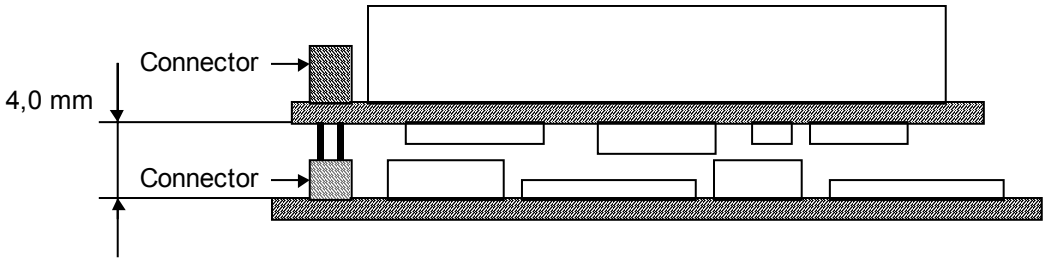


Figure 9: Components fitted on target PCB below HW 86010. Distance between PCBs depend on component heights (here: 4,0 mm)

3.4.2 Connector pinout

Other names	Name	Pin		Pin	Name	Other names
	VXOP	02		01	VXON	
	VXIP	04		03	VXIN	
	MICP	06		05	MICN	
GPIO13	RINGP	08		07	RSTNO	
GPIO14	PWM	10		09	ADC	
	SCL	12		11	SDA	
	GPIO2	14		13	GPIO1	
PCMCLK	GPIO4	16		15	GPIO3	PCMFSYNC
PCMDO	GPIO6	18		17	GPIO5	PCMDI
CS1N	GPIO8	20		19	GPIO7	INT0
	GND	22		21	RSTBI	
GPIO10	DTRI	24		23	RTSI	GPIO9
	TXDI	26		25	RXDO	
	VBATP	28		27	V3P3	
BOOT1	DSRO	30		29	CTSO	BOOT0
GPIO12	RIIO	32		31	DCDIO	GPIO11
	WRLN	34		33	RDN	
	DATA(1)	36		35	DATA(0)	
	DATA(3)	38		37	DATA(2)	
	DATA(5)	40		39	DATA(4)	
	DATA(7)	42		41	DATA(6)	
	ADR(1)	44		43	ADR(0)	
	ADR(3)	46		45	ADR(2)	
	ADR(5)	48		47	ADR(4)	
GPIO16	BNK1	50		49	BNK0	GPIO15

The shown connector pinout directly corresponds to the physical connector pinout, if the HW 86010 is oriented as shown in Figure 2, i.e. pin 1 is located in the top right corner of the connector.

3.4.3 RS-232 interface

3.4.3.1 Signal description

The RS-232 interface uses the following interface signals

Signal	I/O	Description
TXDI	I	Serial data from host to HW 86010
RXDO	O	Serial data from HW 86010 to host
RTSI	I	Hardware handshake from host
CTSO	O	Hardware handshake from HW 86010
DTRI	I	Host ready signal
DSRO	O	HW 86010 ready signal
DCDIO	I/O	Carrier detect modem lead signal
RIIO	I/O	Ring indicator modem lead signal

Caution: All interface signals are 3.3V CMOS level. You must provide an external V.24 line driver, if you want to connect the RS-232 port to a standard V.24 device (PC, modem etc.). Connecting the module to a V.24 line without external line drivers may damage the module.

3.4.3.2 Interface parameters

The HW 86010 is equipped with a fully featured UART.

Parameter	Value
Parity	None
	Even
	Odd
	Mark
	Space
Character size	5 bit
	6 bit
	7 bit
	8 bit
Stop bits	1
	1½ (for 5 bits character size only)
	2
Baud rate	600 Bd
	to 115200 Bd

3.4.4 Voice Interface

3.4.4.1 Interface signals

The voice interface provides connections for microphone and loudspeaker. It uses the following interface signals

Signal	I/O	Description
VXON	O	Analogue speaker output negative
VXOP	O	Analogue speaker output positive
VXIN	I	Analogue microphone input negative
VXIP	I	Analogue microphone input positive
MICBN	O	Microphone bias voltage negative
MICBP	O	Microphone bias voltage positive

3.4.4.2 Interface parameters

Parameter		Value
Microphone interface	Input impedance	10kΩ +/-30%
	Analogue gain Amplification Attenuation	Configurable by firmware 12 steps of +3dB (+/-10%) 7 steps of -2dB (+/-10%)
	Digital attenuation	Configurable by firmware 6 steps of -0,5dB
	MICBP-MICBN	Configurable by firmware 1.62V to 1.98V
	Output current	1mA max.
	Load	200pF max.
Loudspeaker interface	Load	50Ω min. 1000pF (audio frequency range)
	Gain	Configurable by firmware 16 steps of 2dB Maximum gain limited by V3P3
	Power down	20kΩ differential impedance

3.4.4.3 Connection of microphone and speaker

A typical full-differential connection of a microphone is shown in Figure 10. The values of the components must be chosen such that

- The AC coupling capacitors C1 and C2 form together with the input impedance of the pre-amplifier a transfer function with a zero at a frequency low enough to avoid unacceptable ripples in the considered signal bandwidth. The pre-amplifier impedance is 10 kΩ +/-30%.
- A very low frequency pole (below 50 Hz) is formed by the capacitor C4 and the series resistors R1 and R2.
- The microphone biasing current is set such that the required sensitivity target is met. This depends on the microphone characteristics.
- System performance may be further enhanced by an additional capacitor C3 that filters out the peak of the cavity resonance. The value depends on the physical characteristics of the microphone housing.

Component values in Figure 10 are typical for a low impedance microphone (less than 3 kΩ).

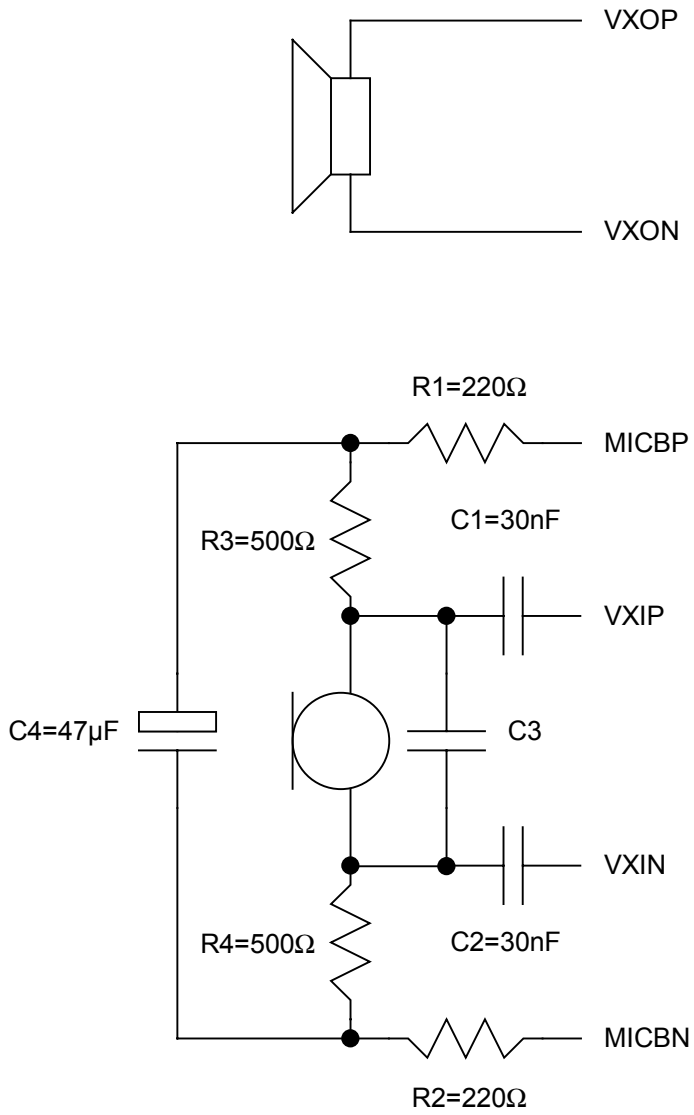


Figure 10: Electrical connection of microphone and loudspeaker

The connection of a loudspeaker is also shown in Figure 10. In power-down mode an impedance of 20kΩ between the differential outputs VXOP and VXON is kept.

3.4.5 ADC/PWM interface

This interface is used to capture and reproduce analogue signals which have a low bandwidth.

3.4.5.1 Signal description

Signal	I/O	Description
ADC	I	Analogue signal input
PWM	O	PWM signal output

3.4.5.2 Analogue to Digital conversion

The ADC input is used to convert an analogue signal into a digital signal.

The applied voltage is restricted to the range 0.0V to 2.5V.

3.4.5.3 Digital to Analogue conversion

The PWM output is a digital pulse-width modulated output. The output signal has a frequency of 6.75 kHz. An analogue signal is retrieved by low pass filtering outside the HW 86010.

Please note that the reference voltage of the PWM output is V3P3. In order to reproduce exactly the analogue input voltage at ADC input, the PWM signal must be converted from V3P3 down to 2.5V prior to low pass filtering.

When the ADC/PWM interface is disabled, the ADC input is ignored and the PWM output is held to 0.0V.

3.4.6 Reset Interface

The reset interface serves the purpose of resetting the HW 86010 and its external peripherals.

3.4.6.1 Signal description

Signal	I/O	Description
RSTBI	I	Reset input, triggers on falling edge
RSTNO	O	Reset output, active low
BOOT0	I	Switches HW 86010 in download mode
BOOT1	I	Switches HW 86010 in download mode

3.4.6.2 External and internal resets

A reset of the HW 86010 may occur in different situations:

- Power-up reset
- Low voltage alarm from internal supervisory circuit
- Initiated by firmware or watchdog
- External reset through RSTBI signal

The DECT module must be able to reliably distinguish an external reset from any other reset (collectively referred to as internal resets). This is achieved through appropriate reset timing.

The host, which initiates the external reset must pull the RSTBI signal down. This will physically reset the DECT module as can be observed on the RSTNO output.

After termination of its internal reset cycle, the HW 86010 will raise the RSTNO signal and firmware program starts. In an early stage of program execution the firmware will test the value of the RSTBI signal. An external reset is indicated by a logical low.

At power-up the HW 86010 is automatically reset by the internal supervisory circuit.

A reset by the host processor (using the RSTBI signal) is needed under the following circumstances:

- to enable a firmware download (see section 3.4.6.5)
- to initiate specific firmware actions (depending on the actual firmware)

If none of these functions are required by the application, the RSTBI pin may be left not connected. In any case, taking provisions for potential firmware downloads in your product is a substantial advantage for the future-proofness of your product.

3.4.6.3 Reset timing (external reset)

In order to make sure that an external reset is detected correctly by the firmware, the host must pull RSTBI down sufficiently long time. The exact timing requirements are indicated in Figure 11.

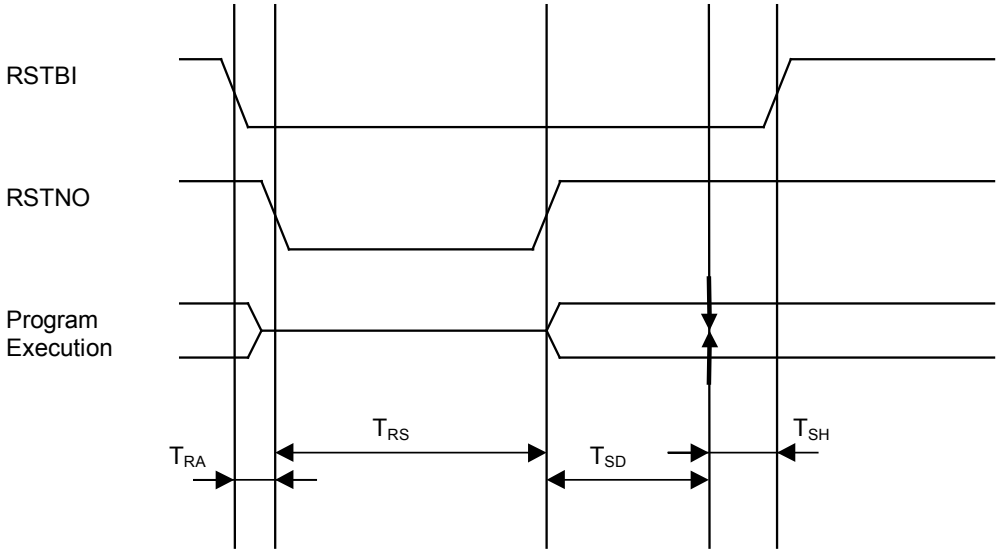


Figure 11: Reset timing

Parameter	min.	max.
T_{RA}		11µs
T_{RS}	100ms	860ms
T_{SD}	18µs	100ms
T_{SH}	100µs	

The host hardware can be sure to generate external reset pulses of sufficient length, if

- either it observes the RSTNO signal and keeps the RSTBI signal LOW at least 100ms after the rising edge of RSTNO, or
- it applies a RSTBI pulse of at least 970ms.

The latter method is simpler but also slower.

T_{RS} depends on component tolerances, temperature and operating voltage. It may be variable.

T_{SD} depends on the firmware implementation and may vary between different firmware versions. However the maximum value of 100ms shall not be exceeded by any firmware version.

3.4.6.4 Short reset

A short reset is a low-active RSTBI pulse that is shorter than the rising edge of the RSTNO signal.

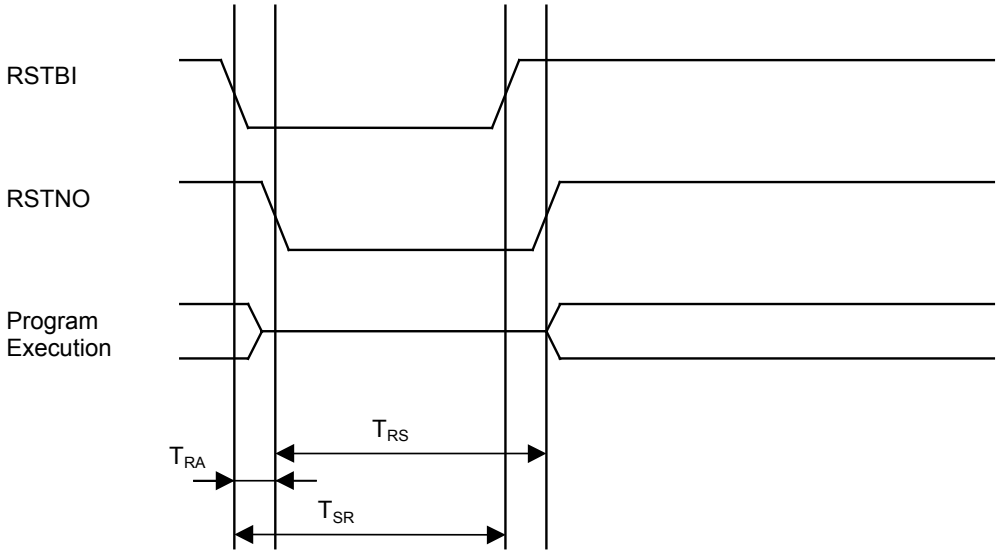


Figure 12: Short reset timing

Parameter	min.	max.
T_{SR}	5ms	50ms

Although it is triggered by the RSTBI signal the firmware of the HW 86010 treats a short reset as an internal reset. The host hardware may use this feature to emulate a power-up reset to the HW 86010.

3.4.6.5 Activation of download mode

During any reset (internal or external) interface signals BOOT0 and BOOT1 overload the normal function of these signals (CTSO and DSRO). They are used to select between normal start of the firmware and firmware download mode.

BOOT0	BOOT1	Function
LOW	LOW	Enable firmware download mode
LOW	HIGH	Reserved for future use
HIGH	LOW	Reserved for future use
HIGH	HIGH	Normal start of the firmware

BOOT0 and BOOT1 are latched at the rising edge of RSTNO. The signals have internal 10 kΩ pull-ups. So they may be left unconnected, if not used. HW 86010 evaluates these signals on every reset (including internal resets). In order to avoid unwanted switches to firmware download mode, the host device shall take care that theses signals are driven low only together with RSTBI driven low.

The evaluation kit HW 86910 contains adapter boards that support firmware download from a standard PC through a normal COM port. The evaluation kit contains further information on firmware download and a loader software for PC Windows-NT/95/98.

3.4.6.6 Precautions to avoid reset problems

The host hardware must assure an appropriate environment that avoids unwanted resets. The reset behaviour is a main source of integration problems and requires specific attention.

Please make sure that the following conditions are fulfilled during operation:

V3P3 must not drop below 2,7V. This will trigger a low voltage reset.

At power-up of the HW 86010 the RSTBI signal should be either high impedance (not connected) or logic HIGH. A logic LOW during power-up may be interpreted as external reset and may result in unwanted mode selection.

If the host hardware is not able to assure the appropriate RSTBI level during power-up, it may use a short reset afterwards to emulate a power-up reset.

DSRO and CTSO are outputs of the HW 86010. The host hardware must never actively drive these signals for any other purpose than entering the download mode.

The external reset is triggered by the falling edge of the RSTBI signal. Make sure that the fall time (90% down to 10% of V3P3) is less than 50ns.

3.4.7 I²C Interface

The I²C interface is a two-wire synchronous serial bus that allows external hardware to be controlled by HW 86010.

3.4.7.1 Signal description

Signal	I/O	Description
SDA	I/O	Serial data of I²C interface
SCL	O	Clock of I²C interface

When used as output, the SDA signal is open drain with internal pull-up.

The SCL signal is a standard (totem-pole) CMOS output.

3.4.7.2 Characteristics of the I²C bus

The I²C bus is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL).

Any I²C system consists in master devices and slave devices. A master is a device that controls the communication, e.g. generates the SCL clock signal.

The HW 86010 can only be operated as master device but not as slave device.

The general concept of the I²C bus allows multiple master devices on the same bus. This is not supported by HW 86010, i.e. it must be the only master device on the bus.

3.4.7.3 Interface parameters

Parameter	Value
Clock rate	43,2 kHz
	86,4 kHz
	172,8 kHz
	345,6 kHz

3.4.7.4 Signal timing

The timing of the I²C bus is shown in Figure 13. The example illustrates a bus transaction containing of one byte sent from the master to the slave followed by one byte sent from the slave to the master.

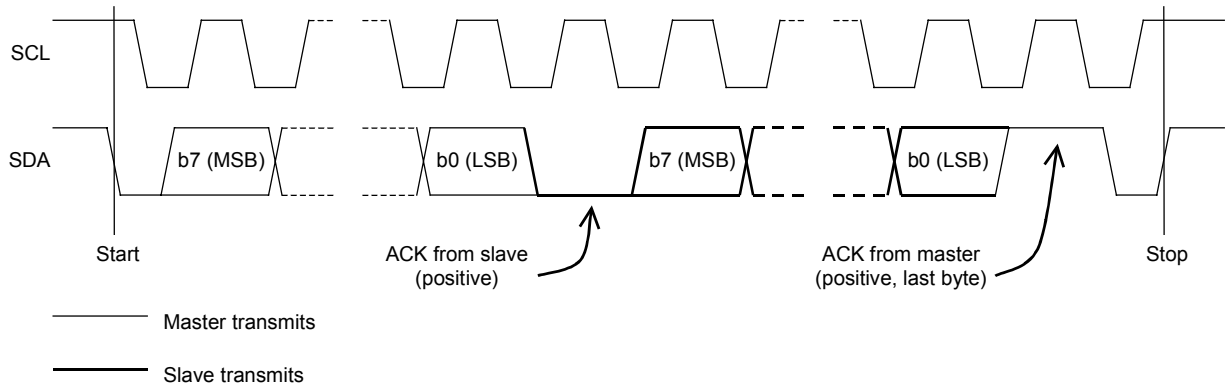


Figure 13 I²C interface signal timing

Data transfer is initiated by the master (HW 86010) when the bus is not busy, i.e. both data and clock lines are logic High. The master generates a Start condition, i.e. a High-to-Low transition of SDA while SCL is High.

Then the master transmits a number of bytes. One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the High period of the clock pulse. The bits are sent in the order MSB first with polarity 0=low, 1=high.

The number of data bytes transferred from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The transmitter must release the SDA line before the receiver can send an acknowledge bit.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte.

As defined by a higher layer protocol depending on the kind of slave device, by sending specific commands the master may initiate a data transfer from the slave. In the example shown in Figure 13 we may assume that such a command was contained in the first byte.

Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable Low during the High period of the

acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge after the **last** byte that has been clocked out of the slave. This is done by the master receiver by holding the SDA line High.

In this event the transmitter must release the data line to enable the master to generate a Stop condition. This is defined as a Low-to-High transition of the data line while the clock is High.

3.4.8 PCM Interface

The PCM interface is used to link the HW 86010 with a variety of dedicated telecommunications controllers. An operating mode compatible with IOM-2 is supported.

3.4.8.1 Signal description

Signal	I/O	Description
PCMCLK	I/O	PCM clock signal
PCMDO	O	Serial data output signal
PCMDI	I	Serial data input signal
PCMFSYNC	I/O	PCM frame sync signal

3.4.8.2 Interface parameters

The PCM interface supports the following configurations

Clock speed	Bit rate	Clocking
4.096 MHz	256 bits per frame	Double clock IOM-2
2.048 MHz	256 bits per frame	Single clock PCM
1.536 MHz	192 bits per frame	Single clock PCM
1.536 MHz	96 bits per frame	Double clock IOM-2

The PCM interface can only access channel 0 of the PCM frame.

It can operate as PCM clock master or slave.

All parameters are controlled by the firmware.

3.4.9 General Purpose I/O

HW 86010 provides 16 general purpose I/O pins GPIO1 to GPIO16. They are enabled by firmware.

These signals are 3.3V CMOS.

3.4.9.1 Signal description

Signal	I/O	Description
GPIO1	I/O	not multiplexed
GPIO2	I/O	not multiplexed
GPIO3	I/O	multiplexed with PCM interface
GPIO4	I/O	multiplexed with PCM interface
GPIO5	I/O	multiplexed with PCM interface
GPIO6	I/O	multiplexed with PCM interface
GPIO7	I/O	multiplexed with Bus interface
GPIO8	I/O	multiplexed with Bus interface
GPIO9	I/O	multiplexed with RS-232 interface
GPIO10	I/O	multiplexed with RS-232 interface
GPIO11	I/O	multiplexed with RS-232 interface
GPIO12	I/O	multiplexed with RS-232 interface
GPIO13	I/O	multiplexed with Ringer interface
GPIO14	I/O	multiplexed with ADC/PWM interface
GPIO15	I/O	multiplexed with BNK0 bus signal
GPIO16	I/O	multiplexed with BNK1 bus signal

3.4.9.2 Usage of GPIO signals

GPIO signals are used by specific firmware functions. Since most GPIO signals are multiplexed with other interface signals, certain restrictions to the usage of GPIO signals apply.

3.4.10 Bus Interface

Purpose of the bus interface is to provide a means for easy access to custom-specific peripherals.

3.4.10.1 Signal description

Signal	I/O	Description
DATA(0-8)	I/O	8-bit data bus
ADR(0-5)	O	6-bit address bus
BNK0, BNK1	O	bank switch signals (2-bit address extension)
RDN	O	Read enable signal, active low
WRLN	O	Write enable signal, active low
CS1N	O	Chip select signal, active low
INT0	I	External interrupt input

This standard 8-bit µC bus is INTEL compatible.

3.4.10.2 Usage of the bus interface

The bus interface may be used for many applications.

The function depends on the firmware.

Please contact Höft & Wessel for more information on firmware customisation.

3.5 Firmware download mode

This section describes, how firmware is downloaded in the HW 86010.

In order to perform firmware download the HW 86010 must be switched into Download Mode.

While in Download Mode the HW 86010 uses a simple download protocol for downloading the firmware via the RS-232 interface.

3.5.1 Entering the Download Mode

The download mode is entered depending on the status of the BOOT0 and BOOT1 signals during reset. See section 3.4.6.5 for details.

3.5.2 Usage of the RS-232 interface

In download mode only signals TXDI and RXDO are used. No flow control is applied.

When the download mode is started, the baud rate of the RS-232 interface is set to 9.600 Bd. However after the first pass of the download protocol the data rate is increased to 115.200 Bd.

3.5.3 Download protocol

Firmware as it is provided by Höft & Wessel consists in two files:

- A loader file (xxx.ld) that is loaded first into the module and provides the mechanisms for loading the firmware into the Flash memory of the module
- A firmware file (xxx.hp) that contains the firmware to be stored in Flash memory

The download protocol consists in two passes. The first pass loads the loader file, the second pass loads the firmware file.

3.5.3.1 Pass one

Step	Action	Note
1	Enter Download Mode	see section 3.4.6.5
2	Initialise RS-232 port	9.600 Bd, 8 data bits, no parity, 1 stop bit
3	Transmit byte 0xAA	StartRequest token
4	Receive byte 0xA1	StartConfirm token
5	Transmit 2 bytes LenLd	Length in bytes of file xxx.ld expressed as 2-byte unsigned. Low byte transmitted first.
6	Receive 2 bytes LenLd	Compare with LenLd from step 5. Only continue if equal. Otherwise stop with error.
7	Transmit byte 0x00	Acknowledgement token
8	Transmit file xxx.ld	Binary transfer of LenLd bytes. In parallel compute a CRC (see section 3.5.3.3)
9	Receive 2 bytes CRC	Low byte transmitted first. Compare with computed CRC from step 8. Only continue if equal. Otherwise stop with error.
10	Transmit byte 0x00	Acknowledgement token
11	continue with pass two	

Any transmit must not pause more than 1 second. Otherwise the HW 86010 may timeout.

If not otherwise noted, any receive must tolerate a pause of 2 seconds before the host timeouts.

If during pass 1 the download procedure stops with error or is interrupted by the host, the previous firmware remains intact in the Flash memory.

3.5.3.2 Pass two

Step	Action	Remark
1	Change baud rate	115.200 Bd, 8 data bits, no parity, 1 stop bit
2	Wait 10 ms	Allow HW 86010 to change baud rate
3	Transmit byte 0xAA	StartRequest token
4	Receive byte 0xA1	StartConfirm token
5	Transmit 4 bytes LenHp	Length in bytes of file xxx.hp expressed as 4-byte unsigned. Low byte transmitted first.
6	Receive 4 bytes LenHp	Compare with LenHp from step 5. Only continue if equal. Otherwise stop with error.
7	Transmit byte 0x00	Acknowledgement token
8	Receive byte 0x00	This confirms that the Flash memory was successfully erased. Step 8 includes erasing the Flash and may take up to 15 seconds. Any return value other than 0 signals an error.
9	Transmit block of file xxx.hp	Binary transfer. The block length is 1024 bytes. If less than 1024 bytes are left to be transmitted, the size of the block is reduced accordingly. Compute a CRC for the block (see section 3.5.3.3)
10	Receive byte 0x00	If there is another value, an error is indicated.
11	Receive 2 bytes CRC	Low byte transmitted first. Compare with computed CRC from step 9. Only continue if equal. Otherwise stop with error.
12	Transmit byte 0x00	Acknowledgement token
13	Repeat steps 9 to 11 until end of file xxx.hp	
14	Start new firmware	Through reset of module

Any transmit must not pause more than 1 second. Otherwise the HW 86010 may timeout.

If not otherwise noted, any receive must tolerate a pause of 2 seconds before the host timeouts.

If during pass 2 the download procedure stops with error or is interrupted by the host, no valid firmware is left in the module. However a firmware download is still possible.

3.5.3.3 Computation of CRC

The following short piece of C-code describes the computation of a CRC for a block of bytes to be applied for firmware download:

```
unsigned short CalculateCRC (
   unsigned char *Block,   /* array of bytes */
   unsigned int BlockLen   /* length of Block in bytes */
)
{
   unsigned short crc = 0; /* CRC initialised with zero */
   unsigned char BitPos;   /* counter for bit level loop */

   while (BlockLen != 0)   /* main loop over all bytes */
   {
      crc ^= ( (unsigned short) *Block++ << 8)
                           /* modulo-2 add a byte */
      for (BitPos=0; BitPos<8; BitPos++)
                           /* loop over all bits of byte */
      {
         if (crc & 0x8000)
           crc = (crc << 1) ^ 0x1021
         else
           crc <<= 1;
                           /* apply generator polynomial */
      }
      BlockLen--;          /* decrement loop counter */
   }
   return crc
}
```

4.0 Specific integration topics

The HW 86010 module has been successfully integrated into many different environments. These projects have shown that certain topics should be treated particularly careful in the product design.

4.1 Type approval issues

A product that uses HW 86010 and is destined for countries of the European Union requires a manufacturer declaration according to the R&TTE directive.

HW 86010 has a type approval according the European CTR 6 standard. This is a mandatory requirement for DECT equipment.

When you integrate HW 86010 in your product, there is no need for doing the complete CTR 6 test again. Although it is not mandatory, Höft & Wessel recommends that you have your product checked in a shortened CTR 6 spot check.

Under the R&TTE directive you will need an EMC test for your product according to EN 300 329 (EMC for DECT equipment) and LVD test.

If you intend to market your product outside the European Union, please check that the respective countries accept the DECT standard. The country-specific regulations for type approval are very different.

If you require support for the type approval process, please address yourself to Höft & Wessel.

4.2 Power supply

The HW 86010 needs two different power supply voltages. The whole digital part runs on 3.3V. Please take care that the 3.3V are stabilised and the ripple is reasonably low (max. 50mV). Note that all digital signals are 3.3V CMOS logic.

In case you must interface to a 5V design take care: Inputs of HW 86010 are **not** 5V tolerant. The module will be damaged, if you connect its digital signals to 5V. However the HIGH level of digital outputs on the HW 86010 is sufficient to safely drive 5V TTL inputs.

The voltage VBATP is used for the RF power amplifier of the module. During the transmission burst it will need a significant current of up to 400 mA. Your power supply must be capable of delivering that current. Figure 7 shows the typical duty cycle.

If VBATP cannot deliver the full current required by the module, the transmission power is too low and this will reduce the coverage range. Due to non-linear distortion the out-of-band radiation is increased. This may cause interference to other radio devices.

Connecting VBATP directly to a 5V supply is not allowed. Although the module will not be damaged, the parameters of the RF signal may violate the limits of the CTR 6 standard.

4.3 Antenna design

The antenna design is among the most important topics of a module integration. It has big influence on the coverage range of your product. With a poor antenna design your product will not have the full range of typical DECT equipment.

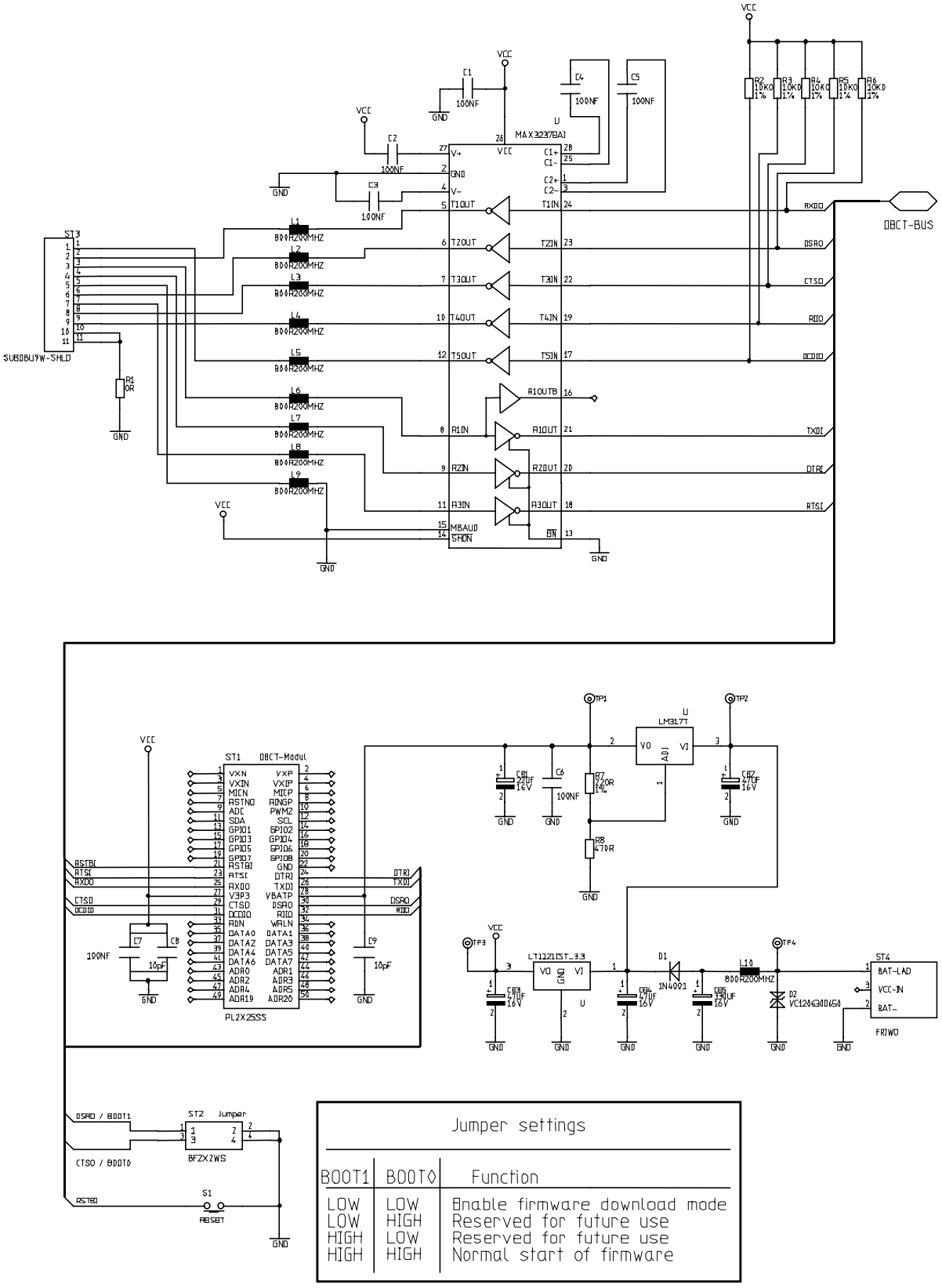
The internal wire antennas of the HW 86010 are usually located inside the housing of a device. Please be aware of the space needed for the antennas, as indicated in Figure 4.

Hints for antenna design:

- The housing of your device should be plastic. If the housing is metal you must not use the internal wire antennas.
- Some plastic materials are conductive, so they behave similar to metal. Particularly avoid graphite (sometimes used for black plastics) and metal paint (sometimes used as EMC shielding).
- Position the module in your device so that the antennas can be kept far from electronic signals and components.
- Be particularly careful with fast signals (like µC bus signals). If they come close to the antennas there is a good chance of crosstalk.
- There should be enough free space around the antennas. If they come very close to the plastic housing there is an influence. You can compensate this influence by reducing the antenna length to some extend. This fine tuning should be done by an RF engineer.
- We recommend that your PCB has a ground plane below the antennas.

Depending on the physical constraints of your device, you may not be able to entirely satisfy all above points. Finding the right compromise for obtaining the optimum RF performance under given space constraints requires in-depth RF experience. Please contact Höft & Wessel if you need any assistance with that topic.

4.4 Schematics diagram example



5.0 Abbreviations

ADC	analogue digital conversion
ARI	access rights identity
BER	bit error rate
CRC	cyclic redundancy checksum
DCE	data communication equipment
DECT	digital enhanced cordless telecommunications
DLC	data link control layer
DNR	DECT serial number
DSP	data service profile
DTE	data terminal equipment
EMC	ETSI manufacturer code
FCS	frame check sequence
FPN	fixed part number
FT	fixed termination
GAP	generic access profile
GFSK	Gaussian frequency<shift keying
GPIO	general purpose I/O
IPEI	international portable equipment identity
IPUI	international portable user identity
ISDN	integrated services digital network
I/O	input / output
LAP	link access protocol
LSB	least significant bit
MAC	medium access control layer
MSB	most significant bit
NLF	new link flag
NWK	network layer
PARI	primary ARI
PARK	portable access rights key
PBX	private branch exchange
PCB	printed circuit board
PCM	pulse code modulation
PIN	personal identity number
PLI	PARK length indicator
PT	portable termination
PWM	pulse width modulation

RF	radio frequency
RFP	radio fixed part
RFPI	radio fixed part identity
RPN	radio fixed part number
SAPI	service access point identity
SARI	secondary ARI
SCL	serial clock
SDA	serial data
SDL	specification description language
SK	subscription key
SMK	subscription master key
TARI	tertiary ARI
TDMA	time division multiple access
UAK	user authentication key
µC	micro controller

6.0 Index